FAIRCHILD
A Schlumberger Company

F6810/F68A10/F68B10 128 x 8-Bit Static Random Access Memory

Microprocessor Product

Description

The F6810 128 x 8-bit static RAM is a byte-organized memory designed for use in bus-organized systems. Fabricated with n-channel, silicon-gate technology, the device is available in three frequency ranges: 1.0 MHz (F6810), 1.5 MHz (F68A10), 2.0 MHz (F68B10). The device, which operates from a single power supply, is compatible with TTL and DTL; it needs no clocks or refreshing because of its static operation.

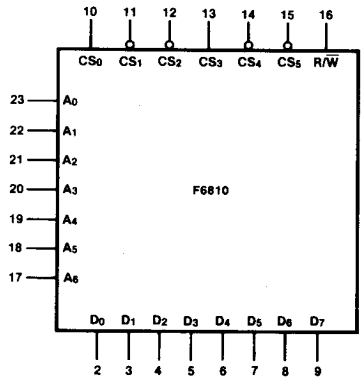
The memory is compatible with the F6800 microcomputer family, providing random storage in byte increments. Memory expansion is provided through multiple chip select inputs.

- **Organized as 128 Bytes of 8 Bits**
- **Static Operation**
- **Bidirectional 3-State Data Input/Output**
- **Six Chip Select Inputs (Four Active LOW, Two Active HIGH)**
- **Single +5 V Power Supply**
- **TTL-Compatible**
- **Maximum Access Time:**
  450 ns for F6810
  360 ns for F68A10
  250 ns for F68B10

Pin Names

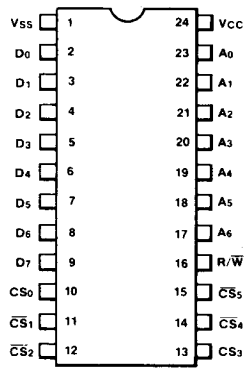
D_0-D_7	Bidirectional Data Bus
A_0-A_6	Address Inputs
CS_0-$\overline{CS}_5$	Chip Select Inputs
$R/\overline{W}$	Read/Write Input

Logic Symbol



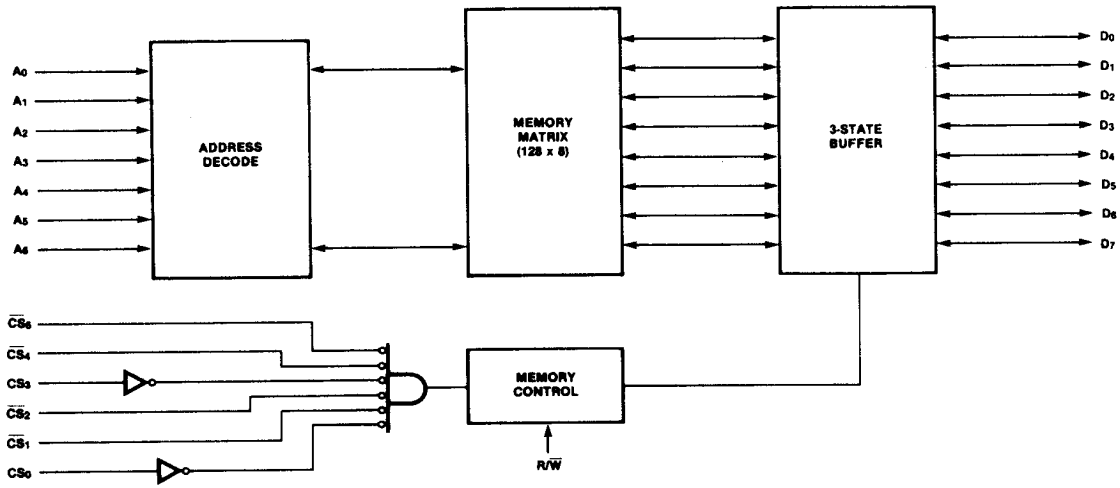
V_{CC} = Pin 24
V_{SS} = Pin 1

Connection Diagram 24-Pin DIP



(Top View)

Block Diagram



Signal Function Descriptions

Mnemonic	Pin No.	Name	Description
Bus Handshake			
A_0-A_6	17-23	Address Bus	Input signal lines containing address to which data is to be written or from which data is to be read
D_0-D_7	2-9	Data Bus	Bidirectional input/output signal lines over which data is read from or written to the device
Chip Control			
CS_0-$\overline{CS}_5$	10-15	Chip Select	Input signal lines that prepare the device for a read or write operation
R/$\overline{W}$	16	Read/Write	Input signal lines that selects a chip read or write operation; a HIGH selects memory read, and a LOW selects memory write
Supply			
V_{SS}	1	Ground	Ground for supply and signals
V_{CC}	24	Supply	+5 V supply voltage

Absolute Maximum Ratings

Supply Voltage	−0.3 V, +7.0 V
Input Voltage	−0.3 V, +7.0 V
Operating Temperature - T_L, T_H	
F6810, F68A10, F68B10	0 °C, +70 °C
F6810C, F68A10C	−40 °C, +85 °C
F6810DM	−55 °C, +125 °C
Storage Temperature Range	−65 °C, +150 °C
Thermal Resistance - θ_{JA}	82.5 °C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

These are stress ratings only, and functional operation at these ratings, or under any conditions above those indicated in this data sheet, is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect device reliability, and exposure to stresses greater than those listed may cause permanent damage to the device.

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input HIGH Voltage	2.0		5.25	V
V_{IL}	Input LOW Voltage	−0.3		0.8	V

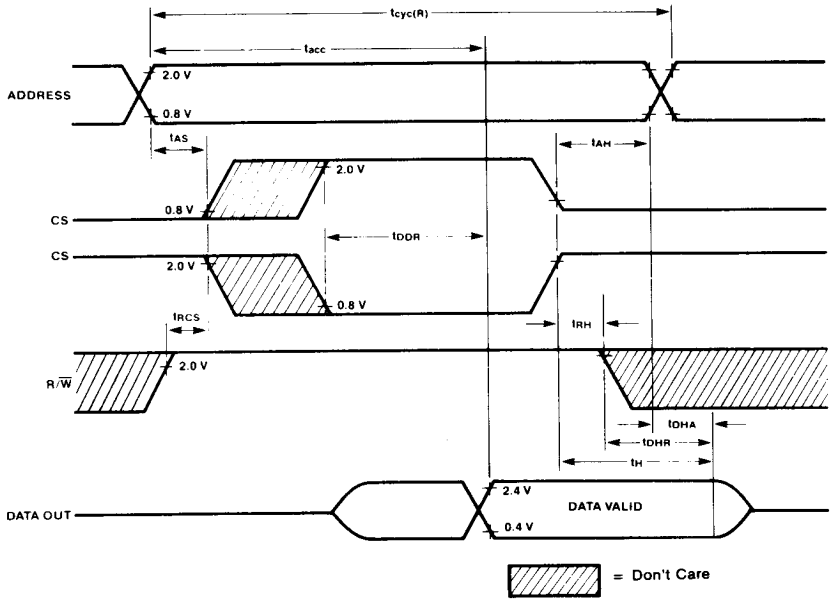
DC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
I_{IN}	Input Current (A_n, R/$\overline{W}$, CS_n, $\overline{CS}_n$)			2.5	μA	V_{IN} = 0 to 5.25 V
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −205 μA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
I_{LO}	Output Leakage Current, 3-State			10	μA	$\overline{CS}$ = 0.8 V or $\overline{CS}$ = 2.0 V, V_O = 0.4 V to 2.4 V
I_{CC}	Supply Current F6810 F68A10, F68B10			80 100	mA	V_{CC} = 5.25 V, all other pins grounded, T_A = 0°C
C_{IN}	Input Capacitance			7.5	pF	f = 1.0 MHz,
C_{OUT}	Output Capacitance			12.5	pF	T_A = 25°C

Bus Timing Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, $T_A = T_L$ to T_H, unless otherwise noted.

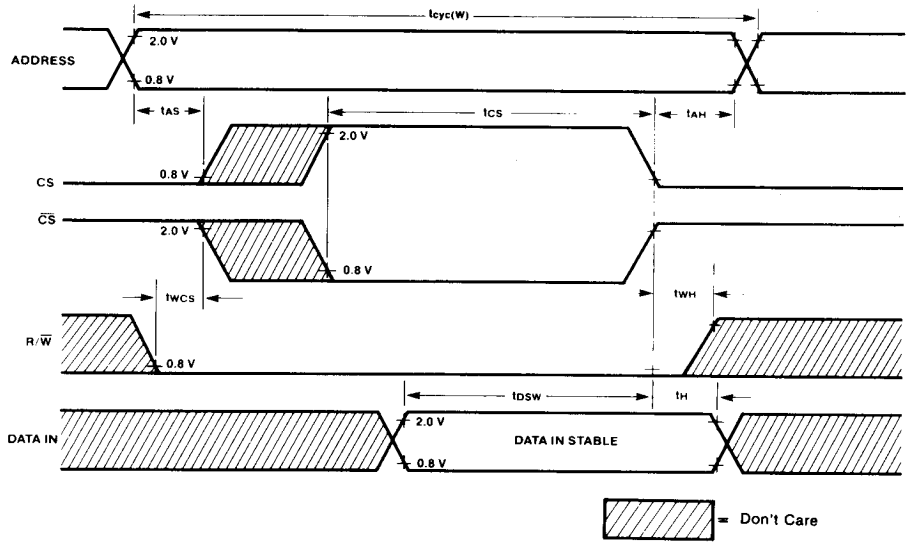
Symbol	Characteristic	F6810		F68A10		F68B10		Unit
		Min	Max	Min	Max	Min	Max	
Read *(Figure 1)*								
$t_{cyc(R)}$	Read Cycle Time	450		360		250		ns
t_{acc}	Access Time		450		360		250	ns
t_{AS}	Address Set-up Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DDR}	Data Delay Time (Read)		230		220		180	ns
t_{RCS}	Read-to-Select Delay Time	0		0		0		ns
t_{DHA}	Data Hold from Address	10		10		10		ns
t_H	Output Hold Time	10		10		10		ns
t_{DHR}	Data Hold from Read	10	80	10	60	10	60	ns
t_{RH}	Read Hold from Chip Select	0		0		0		ns
Write *(Figure 2)*								
$t_{cyc(W)}$	Write Cycle Time	450		360		250		ns
t_{AS}	Address Set-up Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{CS}	Chip Select Pulse Width	300		250		210		ns
t_{WCS}	Write-to-Chip Select Delay Time	0		0		0		ns
t_{DSW}	Data Set-up Time (Write)	190		80		60		ns
t_H	Input Hold Time	10		10		10		ns
t_{WH}	Write Hold from Chip Select	0		0		0		ns

Fig. 1 Read Cycle Timing



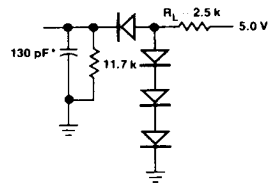
Note
CS and $\overline{CS}$ can be enabled for consecutive read cycles, provided R/$\overline{W}$ remains at V_{IH}.

Fig. 2 Write Cycle Timing



Note
CS and $\overline{CS}$ can be enabled for consecutive write cycles, provided R/$\overline{W}$ is strobed to V_{IH} before or coincident with the address change, and remains HIGH for time t_{AS}.

Fig. 3 Output Load



*Includes jig capacitance

Timing Conditions
The conditions under which the timing characteristics have been determined are as follows:

Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	See *Figure 3*
V_{CC}	5.0 V ±5%
V_{SS}	0
T_A	T_L to T_H, unless otherwise noted

Ordering Information

Speed	Order Code	Temperature Range
1.0 MHz	F6810P,S	0°C to 70°C
	F6810CP,CS	−40°C to +85°C
	F6810DM	−55°C to +125°C
1.5 MHz	F68A10P,S	0°C to +70°C
	F68A10CP,CS	−40°C to +85°C
2.0 MHz	F68B10DM	−55°C to +125°C
	F68B10P,S	0°C to +70°C

P = Plastic package, S = Ceramic package